TB3213

Getting Started with Real-Time Counter (RTC)

Introduction

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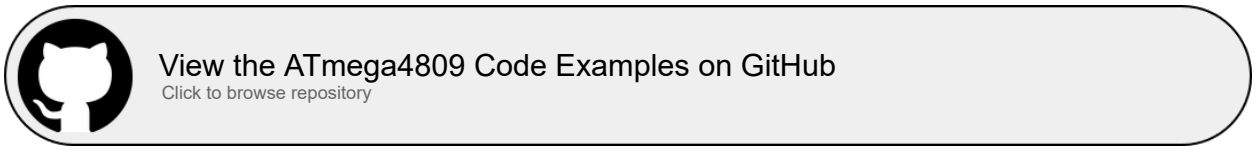
This technical brief describes how the Real-Time Counter (RTC) module works on tinyAVR® 0- and 1-series, megaAVR® 0-series and AVR® DA devices. It covers the following use cases:

- **RTC Overflow Interrupt:**
  Initialize the RTC, enable the overflow interrupt, and toggle an LED on each overflow.
- **RTC Periodic Interrupt:**
  Initialize the RTC PIT, enable the periodic interrupt, and toggle an LED on each periodic interrupt.
- **RTC PIT Wake from Sleep:**
  Initialize the RTC PIT, enable the periodic interrupt, configure device sleep mode, put CPU in Sleep, the PIT interrupt will wake the CPU.

Note: For each use case described in this document, there are two code examples: One bare metal developed on ATmega4809, and one generated with MPLAB® Code Configurator (MCC) developed on AVR128DA48.



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1. Relevant Devices

This section lists the relevant devices for this document. The following figures show the different family devices, laying out pin count variants and memory sizes:

- Vertical migration upwards is possible without code modification, as these devices are pin-compatible and provide the same or more features. Downward migration on tinyAVR® 1-series devices may require code modification due to fewer available instances of some peripherals
- Horizontal migration to the left reduces the pin count and, therefore, the available features
- Devices with different Flash memory sizes typically also have different SRAM and EEPROM

Figure 1-1. tinyAVR® 0-series Overview

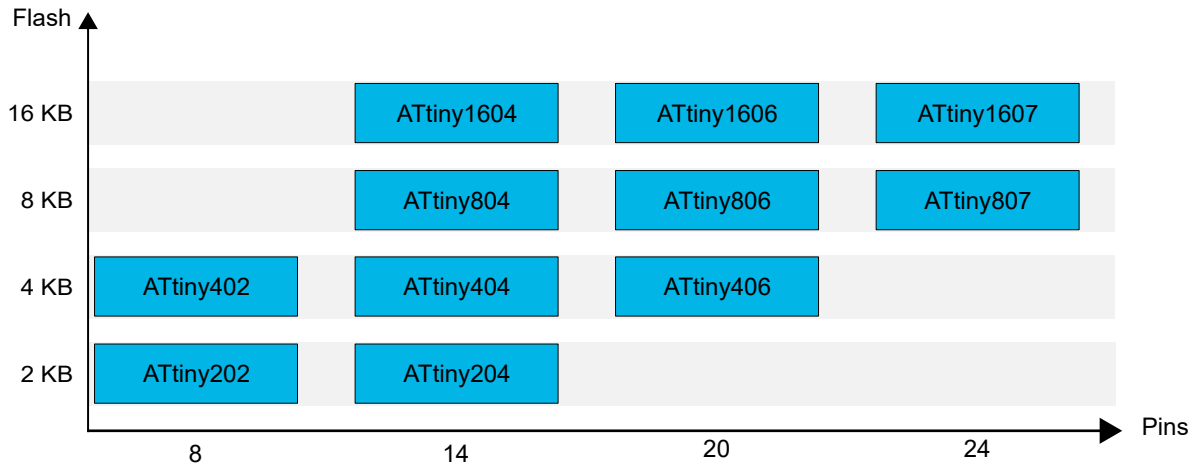


Figure 1-2. tinyAVR® 1-series Overview

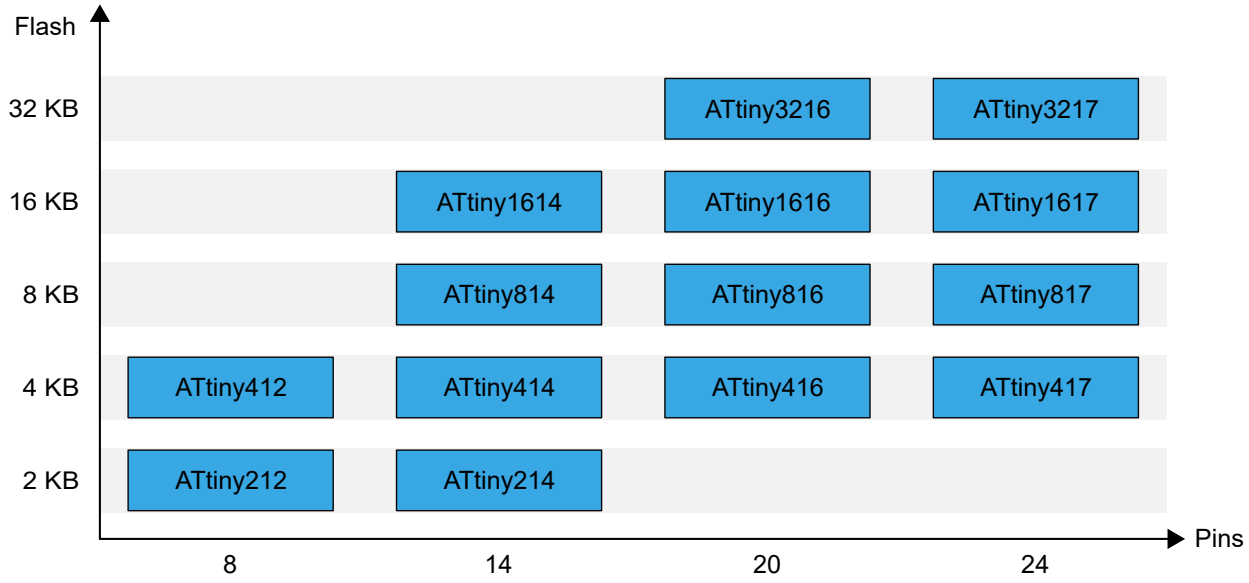


Figure 1-3. megaAVR® 0-series Overview

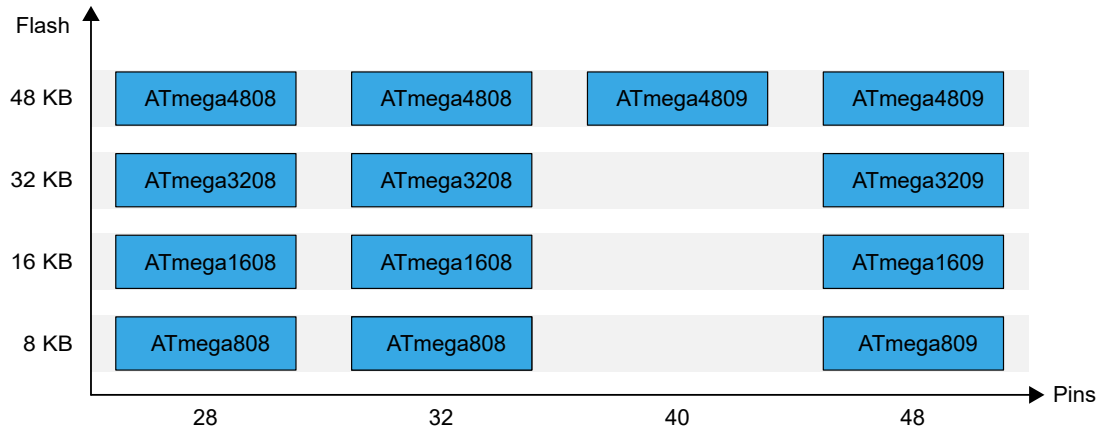
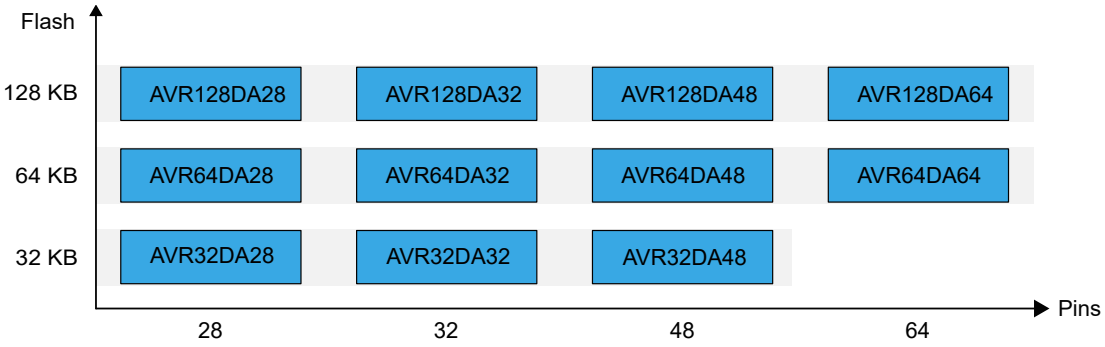


Figure 1-4. AVR® DA Family Overview

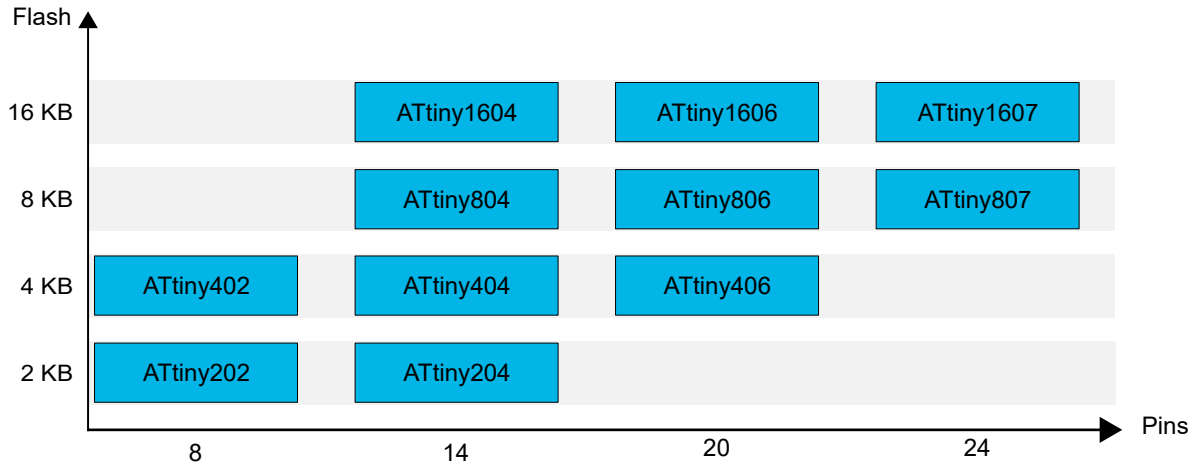


1.1 tinyAVR® 0-series

The figure below shows the tinyAVR® 0-series devices, laying out pin count variants and memory sizes:

- Vertical migration upwards is possible without code modification, as these devices are pin-compatible and provide the same or more features
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1-5. tinyAVR® 0-series Overview



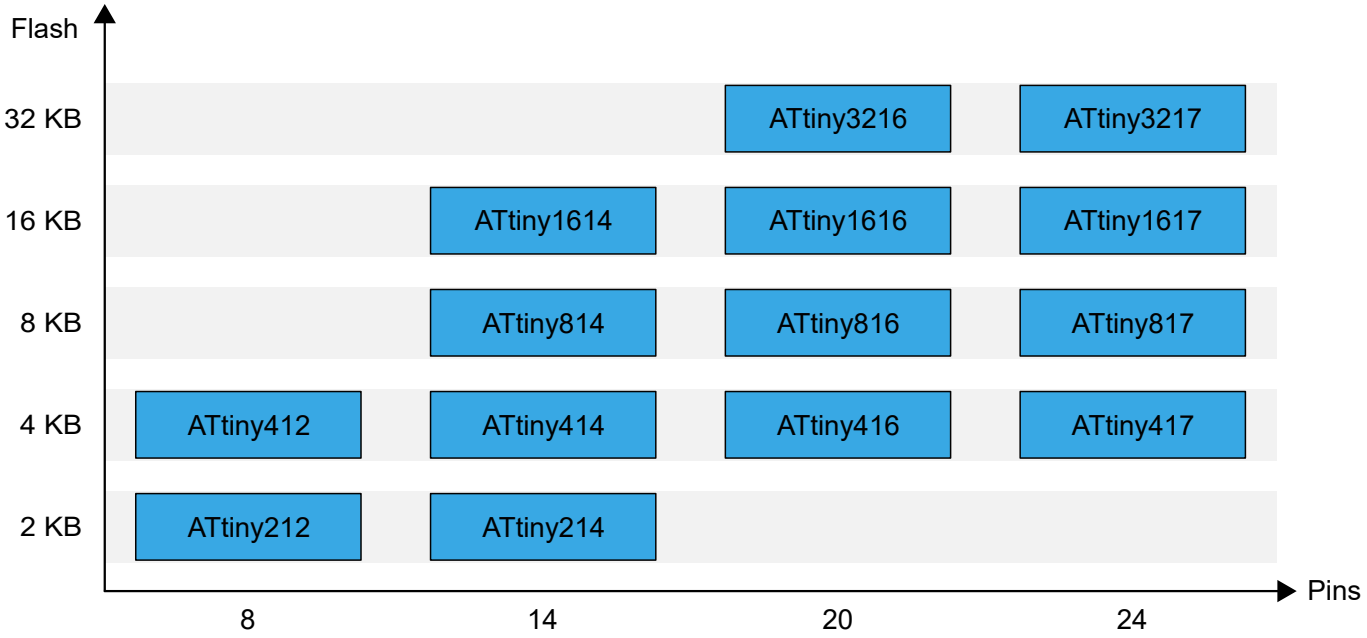
Devices with different Flash memory sizes typically also have different SRAM and EEPROM.

1.2 tinyAVR® 1-series

The following figure shows the tinyAVR 1-series devices, laying out pin count variants and memory sizes:

- Vertical migration upwards is possible without code modification, as these devices are pin-compatible and provide the same or more features. Downward migration may require code modification due to fewer available instances of some peripherals.
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1-6. tinyAVR® 1-series Overview



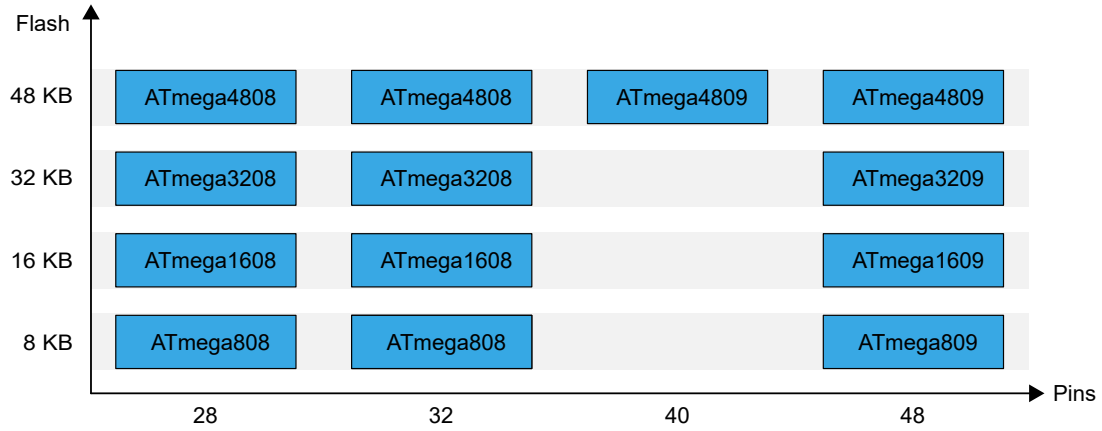
Devices with different Flash memory sizes typically also have different SRAM and EEPROM.

1.3 megaAVR® 0-series

The figure below shows the megaAVR® 0-series devices, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1-7. megaAVR® 0-series Overview



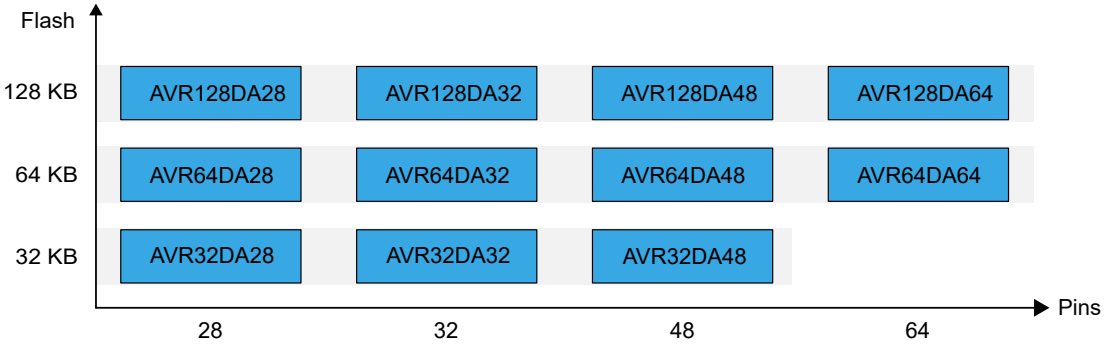
Devices with different Flash memory sizes typically also have different SRAM and EEPROM.

1.4 AVR® DA Family Overview

The figure below shows the AVR® DA devices, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count, and therefore, the available features

Figure 1-8. AVR® DA Family Overview



Devices with different Flash memory sizes typically also have different SRAM.

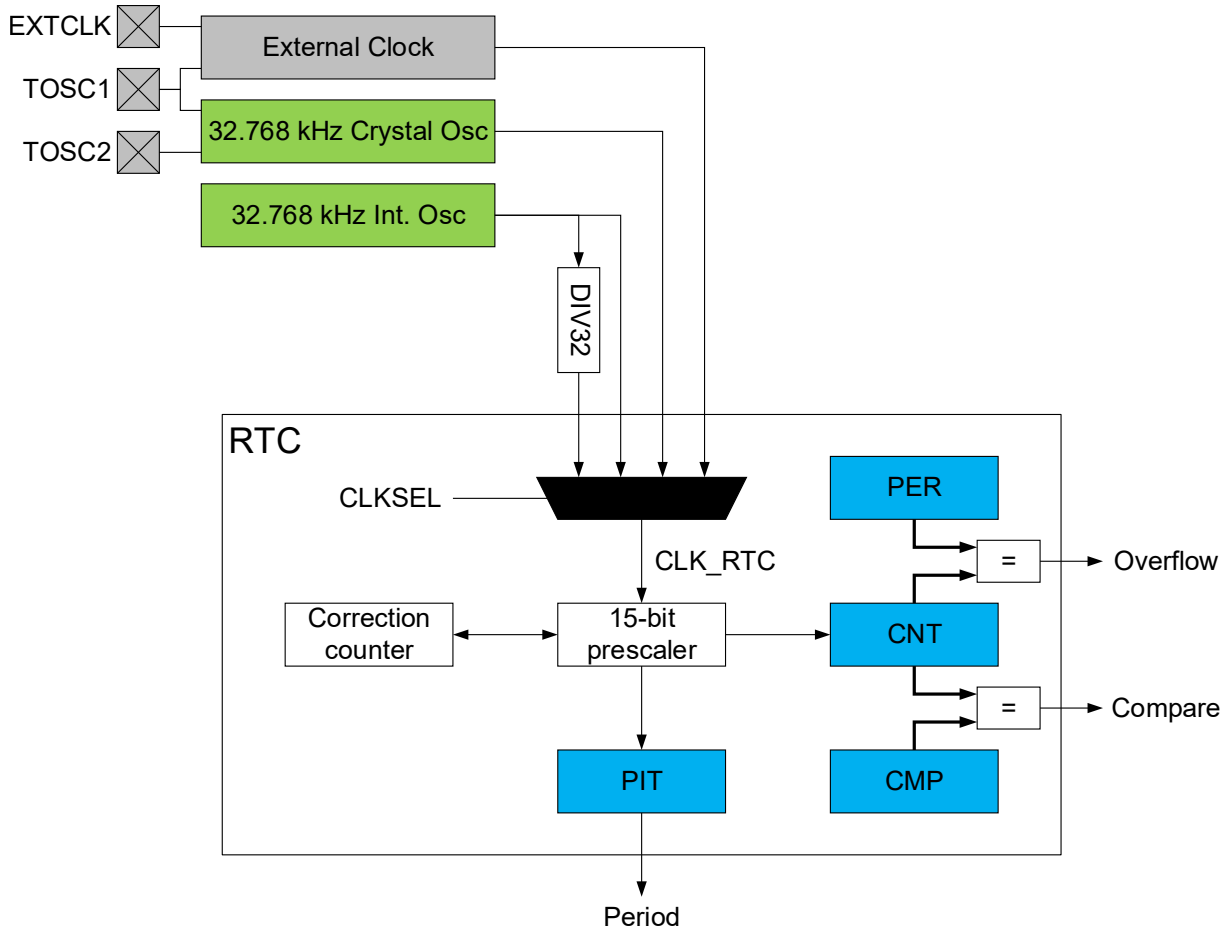
2. Overview

The RTC peripheral offers two timing functions: A Real-Time Counter (RTC) and a Periodic Interrupt Timer (PIT). The PIT functionality can be enabled independently of the RTC functionality.

The RTC counts (prescaled) clock cycles in a Counter register and compares the content of the Counter register to a Period register and a Compare register. The RTC can generate both interrupts and events on compare match or overflow. It will generate a compare interrupt and/or event at the first count after the counter equals the Compare register value, and an overflow interrupt and/or event at the first count after the counter value equals the Period register value. The overflow will also reset the counter value to zero.

Using the same clock source as the RTC function, the PIT can request an interrupt or trigger an output event on every n^{th} clock period ('*n*' can be selected from {4, 8, 16,.. 32768} for interrupts, and from {64, 128, 256,... 8192} for events).

Figure 2-1. Block Diagram



The PIT and RTC functions are running off the same counter inside the prescaler. Writing the PRESCALER bit field in the RTC.CTRLA register configures the period of the clock signal that increments the CNT. The PERIOD bit field in RTC.PITCTRLA selects the bit from the 15-bit prescaler counter to be used as PIT period output.

3. RTC Overflow Interrupt

This code example shows how to use the RTC with overflow interrupt enabled to toggle an LED. The overflow period is 500 ms. The on-board LED will be toggled each time the overflow interrupt occurs.

To operate the RTC, the source clock for the RTC counter must be configured before enabling the RTC peripheral and the desired actions (interrupt requests, output events). In this example, the 32.768 kHz external oscillator is used as the source clock.

To configure the oscillator, first, it must be disabled by clearing the ENABLE bit in the CLKCTRL.XOSC32KCTRLA register:

Figure 3-1. CLKCTRL.XOSC32KCTRLA – Clear the ENABLE Bit

The SEL and CSUT bits cannot be changed as long as the ENABLE bit is set or the XOSC32K Stable (XOSC32KS) bit in CLKCTRL.MCLKSTATUS is high.
To change settings safely: Write a '0' to the ENABLE bit and wait until XOSC32KS is '0' before re-enabling the XOSC32K with new settings.

Bit	7	6	5	4	3	2	1	0
			CSUT[1:0]			SEL	RUNSTDBY	ENABLE
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit 0 – ENABLE Enable
When this bit is written to '1', the configuration of the respective input pins is overridden to TOSC1 and TOSC2. Also, the Source Select (SEL) bit and Crystal Start-Up Time (CSUT) become read-only.
This bit is I/O protected to prevent any unintentional enabling of the oscillator.

```
uint8_t temp;
temp = CLKCTRL.XOSC32KCTRLA;
temp &= ~CLKCTRL_ENABLE_bm;
ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);
```

The user must then wait for the corresponding status bit to become '0':

Figure 3-2. CLKCTRL.MCLKSTATUS – Read XOSC32KS

Bit	7	6	5	4	3	2	1	0
	EXTS	XOSC32KS	OSC32KS	OSC20MS				SOSC
Access	R	R	R	R				R
Reset	0	0	0	0				0

Bit 6 – XOSC32KS XOSC32K Status
The Status bit will only be available if the source is requested as the main clock or by another module. If the oscillator RUNSTDBY bit is set, but the oscillator is unused/not requested, this bit will be 0.

Value	Description
0	XOSC32K is not stable
1	XOSC32K is stable

```
while(CLKCTRL.MCLKSTATUS & CLKCTRL_XOSC32KS_bm)
{
    ;
}
```

Select the external oscillator by clearing the SEL bit in the CLKCTRL.XOSC32KCTRLA register:

Figure 3-3. CLKCTRL.XOSC32KCTRLA – Clear the SEL Bit

Bit	7	6	5	4	3	2	1	0
			CSUT[1:0]			SEL	RUNSTDBY	ENABLE
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit 2 – SEL Source Select
This bit selects the type of external source. It is write protected when the oscillator is enabled (ENABLE = 1).

Value	Description
0	External crystal
1	External clock on TOSC1 pin

```
temp = CLKCTRL.XOSC32KCTRLA;
temp &= ~CLKCTRL_SEL_bm;
ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);
```

Then, enable the oscillator by setting the ENABLE bit in the CLKCTRL.XOSC32KCTRLA register:

```
temp = CLKCTRL.XOSC32KCTRLA;
temp |= CLKCTRL_ENABLE_bm;
ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);
```

Afterward, the user must wait for all registers to be synchronized:

Figure 3-4. RTC.STATUS

Bit	7	6	5	4	3	2	1	0
					CMPBUSY	PERBUSY	CNTBUSY	CTRLABUSY
Access					R	R	R	R
Reset					0	0	0	0

Bit 3 – CMPBUSY: Compare Synchronization Busy
This bit is indicating whether the RTC is busy synchronizing the Compare register (RTC.CMP) in the RTC clock domain.

Bit 2 – PERBUSY: Period Synchronization Busy
This bit is indicating whether the RTC is busy synchronizing the Period register (RTC.PER) in the RTC clock domain.

Bit 1 – CNTBUSY: Counter Synchronization Busy
This bit is indicating whether the RTC is busy synchronizing the Count register (RTC.CNT) in the RTC clock domain.

Bit 0 – CTRLABUSY: Control A Synchronization Busy
This bit is indicating whether the RTC is busy synchronizing the Control A register (RTC.CTRLA) in the RTC clock domain.

```
while (RTC.STATUS > 0)
{
    ;
}
```

The RTC period is set in the RTC.PER register:

Figure 3-5. RTC.PER – Set Period

The RTC.PERL and RTC.PERH register pair represents the 16-bit value, PER. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset `+0x01`. For more details on reading and writing 16-bit registers, refer to *Accessing 16-bit Registers* in the CPU section.
Due to synchronization between the RTC clock and system clock domains, there is a latency of two RTC clock cycles from updating the register until this has an effect. The application software needs to check that the PERBUSY flag in RTC.STATUS is cleared before writing to this register.

Bit	15	14	13	12	11	10	9	8
	PER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	PER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:8 – PER[15:8] Period High Byte
These bits hold the MSB of the 16-bit Period register.

Bits 7:0 – PER[7:0] Period Low Byte
These bits hold the LSB of the 16-bit Period register.

The 32.768 kHz External Crystal Oscillator clock is selected in the RTC.CLKSEL register:

Figure 3-6. RTC.CLKSEL – Clock Selection

Bit	7	6	5	4	3	2	1	0
							CLKSEL[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – CLKSEL[1:0] Clock Select bits
Writing these bits select the source for the RTC clock (CLK_RTC).
When configuring the RTC to use either XOSC32K or the external clock on TOSC1, XOSC32K needs to be enabled, and the Source Select (SEL) bit and Run Standby (RUNSTDBY) bit in the XOSC32K Control A register of the Clock Controller (CLKCTRL.XOSC32KCTRLA) must be configured accordingly.

Value	Name	Description
0x0	INT32K	32.768 kHz from OSCULP32K
0x1	INT1K	1.024 kHz from OSCULP32K
0x2	TOSC32K	32.768 kHz from XOSC32K or external clock from TOSC1
0x3	EXTCLK	External clock from the EXTCLK pin

```
RTC.CLKSEL = RTC_CLKSEL_TOSC32K_gc;
```

To enable the RTC to also run in Debug mode, the DBGRUN bit is set in the RTC.DBGCTRL register:

Figure 3-7. RTC.CLKSEL – Set the DBGRUN Bit

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Debug Run bit

Value	Description
0	The peripheral is halted in Break Debug mode and ignores events
1	The peripheral will continue to run in Break Debug mode when the CPU is halted

```
RTC.DBGCTRL |= RTC_DBGRUN_bm;
```

The RTC prescaler is set in the RTC.CTRLA register. Set the RUNSTDBY bit in RTC.CTRLA to enable the RTC to also run in Standby mode. Set the RTCEN bit in RTC.CTRLA to enable the RTC.

Figure 3-8. RTC.CTRLA – Set the Prescaler, RUNSTDBY Bit, RTCEN Bit

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY	PRESCALER[3:0]				CORREN		RTCEN
Access	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0		0

Bit 7 – RUNSTDBY Run in Standby

Value	Description
0	RTC disabled in Standby sleep mode
1	RTC enabled in Standby sleep mode

Bits 6:3 – PRESCALER[3:0] Prescaler bits
These bits define the prescaling of the CLK_RTC clock signal. Due to synchronization between the RTC clock and system clock domains, there is a latency of two RTC clock cycles from updating the register until this has an effect. The application software needs to check that the CTRLABUSY flag in RTC.STATUS is cleared before writing to this register.

Value	Name	Description
0x0	DIV1	RTC clock/1 (no prescaling)
0x1	DIV2	RTC clock/2
0x2	DIV4	RTC clock/4
0x3	DIV8	RTC clock/8
0x4	DIV16	RTC clock/16
0x5	DIV32	RTC clock/32
0x6	DIV64	RTC clock/64
0x7	DIV128	RTC clock/128
0x8	DIV256	RTC clock/256
0x9	DIV512	RTC clock/512
0xA	DIV1024	RTC clock/1024
0xB	DIV2048	RTC clock/2048
0xC	DIV4096	RTC clock/4096
0xD	DIV8192	RTC clock/8192
0xE	DIV16384	RTC clock/16384
0xF	DIV32768	RTC clock/32768

Bit 0 – RTCEN RTC Peripheral Enable

Value	Description
0	RTC peripheral disabled
1	RTC peripheral enabled

```
RTC.CTRLA = RTC_PRESCALER_DIV32_gc | RTC_RTCEN_bm | RTC_RUNSTDBY_bm;
```

Enable the overflow interrupt by setting the OVF bit in the RTC.INTCTRL register:

Figure 3-9. RTC.INTCTRL – Set the OVF Bit

Bit	7	6	5	4	3	2	1	0
							CMP	OVF
Access							R/W	R/W
Reset							0	0

Bit 0 – OVF Overflow Interrupt Enable
Enable interrupt-on-counter overflow (i.e., when the Counter value (CNT) matches the Period value (PER) and wraps around to zero).

```
RTC.INTCTRL |= RTC_OVF_bm;
```

For the interrupt to occur, the global interrupts must be enabled:

```
sei();
```

The Interrupt Service Routine (ISR) for the RTC overflow will toggle an LED in the example below:

```
ISR(RTC_CNT_vect)
{
    RTC.INTFLAGS = RTC_OVF_bm;
    LED0_toggle();
}
```

Note: Clear the OVF bit from the RTC.INTFLAGS register by writing a '1' to it inside the ISR function.

Tip: The full code example is available in the Appendix section.

View the ATmega4809 Code Example on GitHub
Click to browse repository

An MCC generated code example for AVR128DA48, with the same functionality as the one described in this section, can be found here:

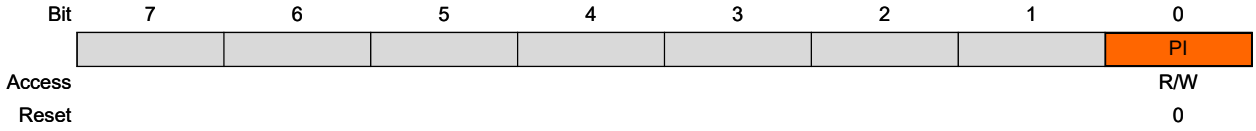
View the AVR128DA48 Code Example on GitHub
Click to browse repository

4. RTC Periodic Interrupt

This code example shows how to use the PIT timing function of the RTC. The on-board LED will be toggled each second when the periodic interrupt occurs.

The source clock configuration for this particular example is the same as for the RTC overflow interrupt example. Enable the periodic interrupt by setting the PI bit in the RTC.PITINTCTRL register.

Figure 4-1. RTC.PITINTCTRL – Set the PI Bit



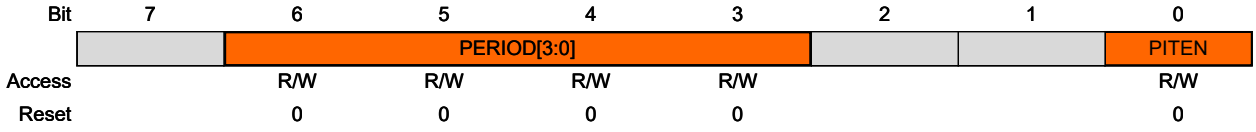
Bit 0 – PI: Periodic Interrupt bit

Value	Description
0	The periodic interrupt is disabled
1	The periodic interrupt is enabled

```
RTC.PITINTCTRL = RTC_PI_bm;
```

The PIT period is set in the RTC.PITCTRLA register. Enable the PIT by setting the PITEN bit in RTC.PITCTRLA.

Figure 4-2. RTC.PITCTRLA – Set the PITEN Bit



Bits 6:3 – PERIOD[3:0]: Period bits
Writing this bit field selects the number of RTC clock cycles between each interrupt.

Value	Name	Description
0x0	OFF	No interrupt
0x1	CYC4	4 cycles
0x2	CYC8	8 cycles
0x3	CYC16	16 cycles
0x4	CYC32	32 cycles
0x5	CYC64	64 cycles
0x6	CYC128	128 cycles
0x7	CYC256	256 cycles
0x8	CYC512	512 cycles
0x9	CYC1024	1024 cycles
0xA	CYC2048	2048 cycles
0xB	CYC4096	4096 cycles
0xC	CYC8192	8192 cycles
0xD	CYC16384	16384 cycles
0xE	CYC32768	32768 cycles
0xF	-	Reserved

Bit 0 – PITEN: Periodic Interrupt Timer Enable bit
Writing a '1' to this bit enables the Periodic Interrupt Timer.

```
RTC.PITCTRLA = RTC_PERIOD_CYC32768_gc | RTC_PITEN_bm;
```

For the interrupt to occur, the global interrupts must be enabled:

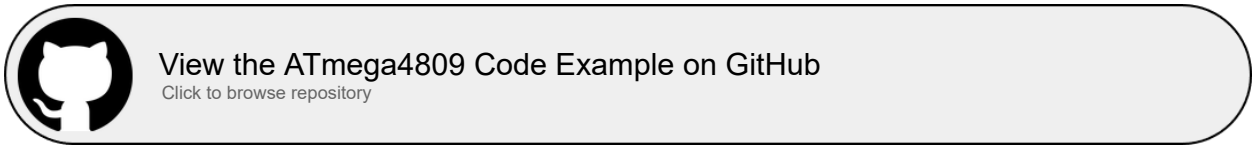
```
sei();
```

The Interrupt Service Routine (ISR) for the RTC PIT will toggle an LED in the example below:

```
ISR(RTC_PIT_vect)
{
    RTC.PITINTFLAGS = RTC_PI_bm;
    LED0_toggle();
}
```

Note: Clear the PI bit from the RTC.PITINTFLAGS register by writing a '1' to it inside the ISR function.

Tip: The full code example is available in the Appendix section.



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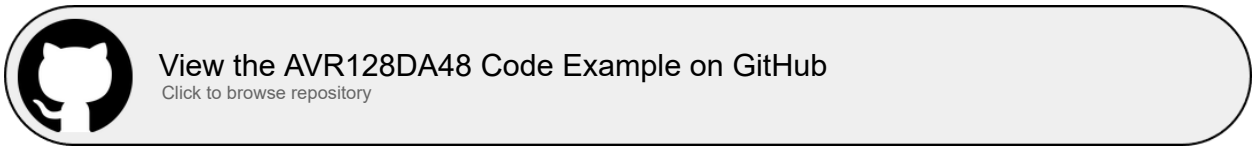

5. RTC PIT Wake from Sleep

This code example shows how to use the PIT timing function of the RTC to wake up the CPU from sleep. The on-board LED will be toggled each second when the periodic interrupt occurs, meaning it will be toggled when the CPU wakes up from sleep.

The sleep mode is configured in the SLPCTRL.CTRLA register. The sleep feature is enabled by setting the SEN bit in SLPCTRL.CTRLA.

Figure 5-1. SLPCTRL.CTRLA – Set the Sleep Mode, SEN Bit

Bit	7	6	5	4	3	2	1	0
						SMODE[1:0]		SEN
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 2:1 – SMODE[1:0] Sleep Mode
Writing these bits selects the sleep mode entered when the Sleep Enable (SEN) bit is written to '1', and the SLEEP instruction is executed.

Value	Name	Description
0x0	IDLE	Idle sleep mode enabled
0x1	STANDBY	Standby sleep mode enabled
0x2	PDOWN	Power-Down sleep mode enabled
other	-	Reserved

Bit 0 – SEN Sleep Enable
This bit must be written to '1' before the SLEEP instruction is executed to make the MCU enter the selected sleep mode.

```
SLPCTRL.CTRLA |= SLPCTRL_SMODE_PDOWN_gc;
SLPCTRL.CTRLA |= SLPCTRL_SEN_bm;
```

The CPU can be put to sleep by calling the following function:

```
sleep_cpu();
```

The PIT interrupt will wake the CPU from sleep. For the interrupt to occur, the global interrupts must be enabled:

```
sei();
```

The Interrupt Service Routine (ISR) for the RTC PIT will toggle an LED in the example below:

```
ISR(RTC_PIT_vect)
{
    RTC.PITINTFLAGS = RTC_PI_bm;
    LED0_toggle();
}
```

Note: Clear the PI bit from the RTC.PITINTFLAGS register by writing a '1' to it inside the ISR function.

Tip: The full code example is available in the Appendix section.

View the ATmega4809 Code Example on GitHub
Click to browse repository

An MCC generated code example for AVR128DA48, with the same functionality as the one described in this section, can be found here:

View the AVR128DA48 Code Example on GitHub
Click to browse repository

6. References

More information about the RTC and PIT operation modes can be found at the following links:

1. AVR128DA48 product page: www.microchip.com/wwwproducts/en/AVR128DA48
2. AVR128DA48 Curiosity Nano Evaluation Kit product page: https://www.microchip.com/Developmenttools/ProductDetails/DM164151
3. AVR128DA28/32/48/64 Data Sheet
4. Getting Started with the AVR® DA Family
5. ATmega4809 product page: www.microchip.com/wwwproducts/en/ATMEGA4809
6. megaAVR® 0-series Family Data Sheet
7. ATmega809/1609/3209/4809 – 48-Pin Data Sheet megaAVR® 0-series
8. ATmega4809 Xplained Pro product page: https://www.microchip.com/developmenttools/ProductDetails/atmega4809-xpro

7. Appendix

Example 7-1. RTC Overflow Interrupt Code Example

```
/* RTC Period */
#define RTC_EXAMPLE_PERIOD            (511)

#include <avr/io.h>
#include <avr/interrupt.h>
#include <avr/cpufunc.h>

void RTC_init(void);
void LED0_init(void);
inline void LED0_toggle(void);

void RTC_init(void)
{
    uint8_t temp;

    /* Initialize 32.768kHz Oscillator: */
    /* Disable oscillator: */
    temp = CLKCTRL.XOSC32KCTRLA;
    temp &= ~CLKCTRL_ENABLE_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    while(CLKCTRL.MCLKSTATUS & CLKCTRL_XOSC32KS_bm)
    {
        ; /* Wait until XOSC32KS becomes 0 */
    }

    /* SEL = 0 (Use External Crystal): */
    temp = CLKCTRL.XOSC32KCTRLA;
    temp &= ~CLKCTRL_SEL_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    /* Enable oscillator: */
    temp = CLKCTRL.XOSC32KCTRLA;
    temp |= CLKCTRL_ENABLE_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    /* Initialize RTC: */
    while (RTC.STATUS > 0)
    {
        ; /* Wait for all register to be synchronized */
    }

    /* Set period */
    RTC.PER = RTC_EXAMPLE_PERIOD;

    /* 32.768kHz External Crystal Oscillator (XOSC32K) */
    RTC.CLKSEL = RTC_CLKSEL_TOSC32K_gc;

    /* Run in debug: enabled */
    RTC.DBGCTRL |= RTC_DBGRUN_bm;

    RTC.CTRLA = RTC_PRESCALER_DIV32_gc  /* 32 */
    | RTC_RTCEN_bm             /* Enable: enabled */
    | RTC_RUNSTDBY_bm;         /* Run In Standby: enabled */

    /* Enable Overflow Interrupt */
    RTC.INTCTRL |= RTC_OVF_bm;
}

void LED0_init(void)
{
    /* Make High (OFF) */
    PORTB.OUT |= PIN5_bm;
    /* Make output */
    PORTB.DIR |= PIN5_bm;
}
```

```
inline void LED0_toggle(void)
{
    PORTB.OUTTGL |= PIN5_bm;
}

ISR(RTC_CNT_vect)
{
    /* Clear flag by writing '1': */
    RTC.INTFLAGS = RTC_OVF_bm;

    LED0_toggle();
}

int main(void)
{
    LED0_init();
    RTC_init();

    /* Enable Global Interrupts */
    sei();

    while (1)
    {
    }
}
```

Example 7-2. RTC Periodic Interrupt Code Example

```
#include <avr/io.h>
#include <avr/interrupt.h>
#include <avr/cpufunc.h>

void RTC_init(void);
void LED0_init(void);
inline void LED0_toggle(void);

void RTC_init(void)
{
    uint8_t temp;

    /* Initialize 32.768kHz Oscillator: */
    /* Disable oscillator: */
    temp = CLKCTRL.XOSC32KCTRLA;
    temp &= ~CLKCTRL_ENABLE_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    while(CLKCTRL.MCLKSTATUS & CLKCTRL_XOSC32KS_bm)
    {
        ; /* Wait until XOSC32KS becomes 0 */
    }

    /* SEL = 0 (Use External Crystal): */
    temp = CLKCTRL.XOSC32KCTRLA;
    temp &= ~CLKCTRL_SEL_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    /* Enable oscillator: */
    temp = CLKCTRL.XOSC32KCTRLA;
    temp |= CLKCTRL_ENABLE_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    /* Initialize RTC: */
    while (RTC.STATUS > 0)
    {
        ; /* Wait for all register to be synchronized */
    }

    /* 32.768kHz External Crystal Oscillator (XOSC32K) */
    RTC.CLKSEL = RTC_CLKSEL_TOSC32K_gc;
```

```
    /* Run in debug: enabled */
    RTC.DBGCTRL = RTC_DBGRUN_bm;

    RTC.PITINTCTRL = RTC_PI_bm; /* Periodic Interrupt: enabled */

    RTC.PITCTRLA = RTC_PERIOD_CYC32768_gc /* RTC Clock Cycles 32768 */
                 | RTC_PITEN_bm; /* Enable: enabled */
}

void LED0_init(void)
{
    /* Make High (OFF) */
    PORTB.OUT |= PIN5_bm;
    /* Make output */
    PORTB.DIR |= PIN5_bm;
}

inline  void LED0_toggle(void)
{
    PORTB.OUTTGL |= PIN5_bm;
}

ISR(RTC_PIT_vect)
{
    /* Clear flag by writing '1': */
    RTC.PITINTFLAGS = RTC_PI_bm;

    LED0_toggle();
}

int main(void)
{
    LED0_init();
    RTC_init();

    /* Enable Global Interrupts */
    sei();

    while (1)
    {
    }
}
```

Example 7-3. RTC PIT Wake from Sleep Code Example

```
#include <avr/io.h>
#include <avr/interrupt.h>
#include <avr/sleep.h>
#include <avr/cpufunc.h>

void RTC_init(void);
void LED0_init(void);
inline void LED0_toggle(void);
void SLPCTRL_init(void);

void RTC_init(void)
{
    uint8_t temp;

    /* Initialize 32.768kHz Oscillator: */
    /* Disable oscillator: */
    temp = CLKCTRL.XOSC32KCTRLA;
    temp &= ~CLKCTRL_ENABLE_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    while(CLKCTRL.MCLKSTATUS & CLKCTRL_XOSC32KS_bm)
    {
        ; /* Wait until XOSC32KS becomes 0 */
    }

    /* SEL = 0 (Use External Crystal): */
```

```
    temp = CLKCTRL.XOSC32KCTRLA;
    temp &= ~CLKCTRL_SEL_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    /* Enable oscillator: */
    temp = CLKCTRL.XOSC32KCTRLA;
    temp |= CLKCTRL_ENABLE_bm;
    /* Writing to protected register */
    ccp_write_io((void*)&CLKCTRL.XOSC32KCTRLA, temp);

    /* Initialize RTC: */
    while (RTC.STATUS > 0)
    {
        ; /* Wait for all register to be synchronized */
    }

    /* 32.768kHz External Crystal Oscillator (XOSC32K) */
    RTC.CLKSEL = RTC_CLKSEL_TOSC32K_gc;

    /* Run in debug: enabled */
    RTC.DBGCTRL = RTC_DBGRUN_bm;

    RTC.PITINTCTRL = RTC_PI_bm; /* Periodic Interrupt: enabled */

    RTC.PITCTRLA = RTC_PERIOD_CYC32768_gc /* RTC Clock Cycles 32768 */
                 | RTC_PITEN_bm; /* Enable: enabled */
}

void LED0_init(void)
{
    /* Make High (OFF) */
    PORTB.OUT |= PIN5_bm;
    /* Make output */
    PORTB.DIR |= PIN5_bm;
}

inline void LED0_toggle(void)
{
    PORTB.OUTTGL |= PIN5_bm;
}

ISR(RTC_PIT_vect)
{
    /* Clear flag by writing '1': */
    RTC.PITINTFLAGS = RTC_PI_bm;

    LED0_toggle();
}

void SLPCTRL_init(void)
{
    SLPCTRL.CTRLA |= SLPCTRL_SMODE_PDOWN_gc;
    SLPCTRL.CTRLA |= SLPCTRL_SEN_bm;
}

int main(void)
{
    LED0_init();
    RTC_init();
    SLPCTRL_init();

    /* Enable Global Interrupts */
    sei();

    while (1)
    {
        /* Put the CPU in sleep */
        sleep_cpu();

        /* The PIT interrupt will wake the CPU */
    }
}
```

8. Revision History

Document Revision	Date	Comments
C	02/2021	Updated the GitHub repository links, the *References* section, and the use cases sections. Added the *AVR® DA Family Overview* section. Added MCC versions for each use case, running on AVR128DA48. Other minor corrections.
B	12/2019	A write to the CCP registers is replaced by the `ccp_write_io()` function in the code.
A	05/2019	Initial document release.

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